REMARKS

Claims 1-10, 12-23, 25-26 and 51-79 are now pending in the application. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the remarks contained herein.

REJECTIONS UNDER 35 U.S.C. § 103

Claims 1-10, 14-23, 51-56, 60-69 and 73-79 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Jaggar (U.S. Pat. No. 5,701,493) in view of Miller et al. (U.S. Pat. No. 5,809,528). Claims 1-10, 14-23 and 51-79 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Jaggar (U.S. Pat. No. 5,701,493). These rejections are respectfully traversed.

Applicants respectfully submit that Jaggar, either alone or in combination with Miller, fails to show, teach, or suggest a plurality of address encoders, a respective one of the plurality of address encoders for each of the input ports, each of the address encoders to provide an encoded address for accessing one of the memory locations. With respect to claim 1, Applicants respectfully note that the Examiner acknowledges that Jaggar fails to disclose this limitation, and instead relies on Miller to make up for the deficiencies of Jaggar. (See Page 3, Lines 19-20 of the Office Action mailed August 15, 2008). The Examiner later alleges that the plurality of address encoders would be obvious in view of the common address encoder of Jaggar.

As shown in an exemplary embodiment in FIG. 4 of the present application, a register file 206 includes a register file memory unit 400 and a plurality of address encoders including, for example, address encoders 402_1, 402_2, 4023, 402_4, 410_1, and

410_2. Each of the address encoders receives a plurality of inputs. For example, the address encoder 402_1 receives a processor mode input and a srcl.index input. In other words, each of the inputs to the register file memory unit 400 includes a corresponding address encoder.

As best understood by Applicants, Jaggar does not disclose a plurality of address encoders as recited in claim 1. For example, with respect to claim 11, the Examiner alleges that Jaggar discloses "an address encoder to provider an encoded address," relying on "the combination of components 12-20 in Fig. 8." Applicants respectfully note that FIG. 8 of Jaggar does not disclose a plurality of address encoders as claim 1 recites. Instead, as best understood by Applicants, FIG. 8 of Jaggar discloses a single alleged address encoder (i.e. the components 12-20) for all of the registers.

The Examiner alleges that providing a plurality of address encoders as claim 1 recites would be obvious to one skilled in the art "simply by duplicating the common address encoder taught by...Jaggar at both input ports." Applicants respectfully disagree and submit that Jaggar teaches away from such a duplication. For example, the alleged encoder of Jaggar receives all register addresses and processor modes at the same encoder and communicates over a single common bus 4. Accordingly, there would be no advantage whatsoever in merely "duplicating" the alleged encoder of Jaggar. Instead, the encoder, as well as the communication bus, would necessarily have to be **modified** in order to justify simple duplication. In other words, there are inherent structural differences in the common encoder of Jaggar.

For example, the Examiner further alleges that modifying Jaggar to simply duplicate the common encoder "increases the overall performance of the data processing system by providing the encoded addresses for all inputs in parallel compared to one by one." Applicants respectfully disagree and submit that duplicating the encoder, without also modifying the encoder and the bus structure of Jaggar, would not improve performance. Instead of one common encoder that converts all addresses and processor modes to encoded addresses, multiple encoders would be converting all address and processor modes to encoded addresses and communicating the encoded addresses over the same common bus. The resulting unnecessary redundancy and increased bus traffic would not increase the performance of Jaggar. Accordingly, Applicants respectfully submit that Jaggar teaches away from simply duplicating the same common address encoder.

Further, Applicants respectfully submit that Miller fails to make up for the deficiencies of Jaggar. For example, the Examiner cites Column 6, Lines 23-35 and element 102 in FIG. 2A in support of the allegation that Miller discloses "having N address encoders one for each input." Applicants respectfully disagree and submit that Miller discloses, at best, the same two encoders associated with all of the inputs.

More specifically, Applicants respectfully note that the cited portions of Miller fail to disclose **a respective one of the plurality of address encoders for each of the input ports**. In other words, Applicants' claim limitation requires that each input port has its own address encoder, which is implicit in the term "respective." In contrast, all of the input ports of Miller appear to share the same encoders.

For example, FIG. 2A of Miller discloses two entry address encoders 102 and 123 and a register stack 110. The register stack 110 includes 32 registers and corresponding input ports. Applicants respectfully note that both of the address encoders 102 and 123 communicate with all 32 registers **via the same address buses 218 and 220**. Accordingly, this structure is not analogous to a respective one of a plurality of address encoders for each of the input ports.

In view of the foregoing, Applicants respectfully submit that claim 1, as well as its dependent claims, should be allowable for at least the above reasons. Claims 14, 51, 64, 74, and 78, as well as their corresponding dependent claims, should be allowable for at least similar reasons.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

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